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Question Paper Code : 41201

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2015.

Third Semester

Electronics and Communication Engineering

EC 1201 — DIGITAL ELECTRONICS

(Regulation 2008)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Define bit, byte and nibble.

2. Find the complement of $A\overline{B} + \overline{B}C + C\overline{D}$.

3. Draw the inverter logic circuit using n-channel MOS devices.

4. What is totem-pole output?

5. How is the overflow condition detected in signed binary number addition?

6. Implement the Boolean function $F(x, y, z) = \Sigma(1, 2, 4, 7)$ using a suitable decoder.

7. How does JK flip flop differ from an S-R flip flop in its basic operation?

8. Mention any four applications of shift registers.

9. Differentiate ROM and RAM.

10. Differentiate PLA and PAL.

PART B — (5 × 16 = 80 marks)

11. (a) (i) Convert the following decimal numbers to their heradecimal equivalent. (8)

(1) 14_{10}

(2) 80_{10}

(3) 3000_{10}

(4) 2500_{10}

(ii) Explain the canonical and standard forms of boolean expression with examples. (8)

Or

(b) (i) Describe the basic laws of Boolean algebra with sample. (8)

(ii) Write the steps for simplifying a logic expression using a Karnaugh map. (8)

12. (a) Explain the construction and operation of DTL and TTL NAND gate. Also mention the characteristics of DTL and TTL families.

Or

(b) (i) Explain CMOS NAND and NOR gate operation. (8)

(ii) Explain the working of tristate logic. (8)

13. (a) Implement the following boolean function with an 8 × 1 multiplexer. $F(A, B, C, D) = \Sigma(0, 3, 5, 6, 8, 9, 14, 15)$.

Or

(b) (i) Design the BCD to excess-3 code converter circuit using logic gates. (10)

(ii) A 3-bit message need to be transmitted together with an even parity bit. Design a 3-bit even parity generator circuit for this data transmission. (6)

14. (a) (i) Design a synchronous decade counter to count in the following sequence. 1, 0, 2, 3, 4, 8, 7,6, 5. (8)

(ii) What is sequential circuit? Explain Ş-R and J K flip flop. (8)

Or

(b) (i) Draw and explain 4-bit synchronous up/down counter. (8)

(ii) Design a serial 2's complementer with a shift register and a flip-flop. The binary number is shifter out from one side and its 2's complement shifted into the other side of the shift register. (8)

15. (a) (i) Explain the organization of ROM. Discuss the different types of ROM. (10)

(ii) Compare SRAM and DRAM. (6)

Or

(b) Show and explain the structure of different programmable logic devices. Discuss their merits and demerits.
